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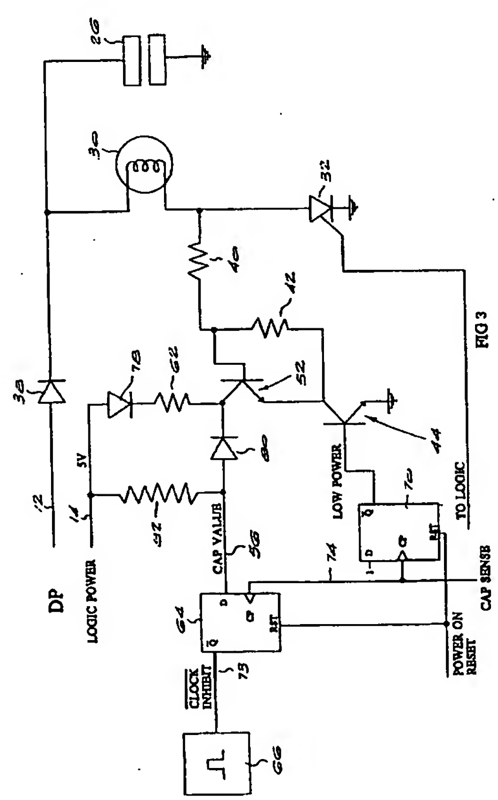
(54) Testing circuit.

(57) A testing circuit is provided for testing the operability both of a load (30) and of a capacitor (26) incorporated into a main detonator circuit and arranged to discharge into the load for detonation thereof. A test pulse is generated at a central controller to which a ring of detonators is connected on a harness. The test pulse is routed via the harness for storage in the capacitor. A controlled switch (44) is operated to allow the capacitor to discharge into the load. A transistor (52) is operated by the discharge signal, the transistor having an output for delivering a discharge value signal (56) in response to the discharge signal remaining above or falling below a threshold value. The discharge value signal is latched and is in turn used to inhibit a local oscillator (66). The inhibited signal from the oscillator is routed back to the controller so as to indicate a fault either in the capacitor (26) or in the load (30).



EP 0 611 944 A1

BACKGROUND OF THE INVENTION

This invention relates to a testing circuit for testing the op rability of a load and a charg storag d vice arranged to discharge into the load.

South African patent 90/7794 filed in the name of the applicant is directed towards timing apparatus for activating a number of electronic detonators at predetermined time intervals. The central control and programming unit is linked to a series of the electronic detonators by means of a bidirectional harness, which is arranged in a loop. In order to ensure that spurious signals do not activate the detonators, a number of safety features have been incorporated into the timing apparatus. One such safety feature is the provision of separate logic and detonator circuits having separate lines from the central controller. The logic circuit is used to power up the detonator logic, and the separate detonator circuit is used to energize a charge storage device, such as a capacitor, just prior to initiation of the blasting sequence. By providing separate circuits, the logic circuitry can be tested in full without danger of the testing signals activating the electronic detonator circuit.

One disadvantage of the testing procedure described in South African patent 90/7794 is that it does not extend to testing of the detonator circuit, and especially the capacitor or the load.

SUMMARY OF THE INVENTION

According to a first aspect of the invention there is provided a testing circuit for testing the operability both of a load and of a charge storage device incorporated into a main circuit and being arranged to discharge into the load for detonation of the load, the testing circuit comprising:

a) signal routing means for routing a test signal from a signal generator for storage in the charge storage device;

b) discharge means for allowing the charge storage device to provide a discharge signal by discharging through the load the charge derived from the test signal;

c) monitoring means for monitoring at least one of the parameters of the discharge signal, and

d) inhibiting means responsive to the monitoring means for inhibiting operation of the main circuit in the event of at least one of the monitored parameters falling outside predetermined limits, the limits being determined with reference to the operability both of the load and of the charge storage device.

Preferably, the monitoring means comprises a first switch which is arranged to be operated by the discharge signal, the first switch receiving a monitoring signal a predetermined time after the test signal, and having an output for delivering a discharge value signal in response to the discharge signal falling below a threshold value which operates the first switch.

Conveniently, the inhibiting means includes latching means for latching the output from the first switch.

The discharge means typically includes a second switch connected along a discharge path, and control means for controlling operation of the second switch, the control means being arranged to open the second switch once the testing circuit has operated, thereby preventing further discharge of the charge storage device along the discharge path.

The testing circuit typically is incorporated into an electronic detonator, which is linked, together with similar detonators, to a central controller via a harness. Both the test signal and the monitoring signal may be generated at the controller and transmitted via respective separate detonator power and logic power lines.

According to a further aspect of the invention there is provided a method of testing the operability both of a load and of a charge storage device incorporated in a main circuit and arranged to discharge into the load, the method including the steps of

a) generating a first test signal;

b) storing the first test signal in the charge storage device;

c) providing a discharge signal by allowing the charge storage device to discharge via the load;

d) monitoring at least one of the parameters of the discharge signal; and

e) inhibiting the operation of the circuit in the event of at least one of the monitored parameters falling outside predetermined limits.

Conveniently, the test signal is of such a magnitude and duration that it is not capable of activating or detonating the load on discharging through the load.

The parameters which are monitored may be time and/or magnitude parameters, and relate to the rate of discharg of the charg storage device, th rat of discharge b ing a function of an RC time constant, where C is the capacitance of th charg storag devic and R includ s the resistance of th l ad. Magnitud parameters may b monitored at a pred termined sampling tim , wh reas time parameters may be monitored at a pred t rmined magnitud thresh ld.

Conv niently, the meth d includes th st ps of allowing th discharge signals to operate a first switch,

g nerating a m nitoring signal and supplying it to the first switch, a pred termined time after th first test signal, and monitoring a discharge valu signal as an output from th switch.

The main circuit typically forms part f an l ctronic d tonator, and the method conv niently includes th step of programming th electronic detonator with timing signals from a remot controller in the vent of the monitored parameters falling within predetermined limits, charging the charge storage device from the remote controller and allowing the charge storage device to detonate the load.

An embodiment of the invention will now be described by way of example only and with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1	shows a schematic block diagram of an electronic detonator;
Figure 2	shows a simplified circuit diagram of a testing circuit of the invention for testing components of the detonator of Figure 1;
Figure 3	shows a more detailed circuit diagram of the testing circuit of Figure 2;
Figure 4	shows a waveform diagram illustrating the sequence of the operation of the simplified circuit of Figure 2;
Figure 5	shows a waveform diagram illustrating the sequence of the operation of the more detailed circuit of Figure 3;
Figure 6	shows a truth table indicating various fault conditions which can arise.

DESCRIPTION OF THE EMBODIMENT

In Figure 1, an electronic detonator 10 is illustrated. The electronic detonator is similar to the delay devices described and illustrated in South African patent 90/7794. A harness 11 comprises a detonator power line 12, a logic power line 14, serially connected prog A and prog B lines 16 and 18 and a ground line 20, all of which interconnect the individual electronic detonators 10.

The opposite ends of the harness terminate at a central controller 21 which provides timing, testing and powering up signals. As is clear from Figure 1, there are two independent circuits, one being constituted by the logic power line 14 and the prog A and prog B lines 16 and 18. The other circuit, the main circuit, is constituted by the detonator power line 12, with the ground line 20 being common to both circuits. The logic power line 14 is connected via a diode 22 to logic circuitry 24 which forms the heart of the electronic detonator. The prog A and prog B lines 16 and 18 are arranged to deliver timing signals in serial form from the central controller to the logic circuitry 24. The detonator power line 12 is only powered up when the entire system is being armed just prior to final detonation.

The detonator power line 12 is arranged to charge an energy storage device which is typically in the form of a 35 V 100 μF capacitor 26. The capacitor 26 is in turn arranged to discharge through a load 30, which is typically a one ohm series resistor made from a high resistance wire compound which generates heat. The resistor is surrounded by a match-head-type chemical compound which ignites on heating of the resistor, thereby igniting the explosive compounds and detonating the main charge. The logic circuitry 24 controls the operation of the switch 32, closure of which will cause the capacitor 26 to discharge through the load 30.

Once the logic circuitry has been programmed with timing signals by the prog A and prog B lines 16 and 18 and testing has taken place, the detonator power line is raised so as to charge the capacitor 26.

Lowering of the detonator power line serves as a signal for the logic circuitry 24 to commence timing. All the harness lines are isolated from the central controller on lowering of the detonator power line, and the logic circuitry is thereafter powered from the capacitor 26 via a diode 34. Once the time period stored in the logic circuitry has counted down to zero, a signal from the logic circuitry 24 closes the switch 32, thereby causing the capacitor 26 to discharge into the load 30, so as to detonate it.

As the various electronic detonators are moved from one site to another, underground vibrations and similar disturbances may cause the solder connections which hold the load or anchor the capacitor 26 to vibrate loose, thereby resulting in the electronic detonator not functioning correctly or at all. In the electronic detonator which is being developed by the applicant, reliabilities of one in ten thousand are being aimed at. It is thus desirable to be able to test, prior to the blast, that the capacitor and the load are functioning properly and are conn cted correctly.

Ref rring n w to Figures 2 and 4, before th logic pow r line 14 is pow red up, a test puls 36 is routed from th central controll r along th d tonator pow r lin 12. The test puls 36 has a durati n of approximately 0.1 second and a magnitud of 2 volts. Assuming that th diode 28 is an ideal diod , the capacitor will charge up to 2 volts, as is shown at 38. On terminati n of the test pulse 36, the capacitor will discharg through the

load and through resistors 40 and 42 to ground via a low power switch 44, which is in th closed positi n. The discharg signal 46 is indicated at node 53 and is a proportion of the signal at node 48.

Naturally, the rate of discharge will be a functi n of an RC time constant, wh re C is th capacitance of the capacitor 26 and R is th sum of the resistances of the load 30 and the resistors 40 and 42.

At a predetermined time S after the test pulse 36 has gone low, the logic power line 14 is raised, as is shown at 50, thereby providing a monitoring signal 51.

In the event of the magnitude of the discharge voltage 46 still exceeding the bias threshold of transistor 52 at node 53, the transistor 52 will remain on and a capacitor value signal 54 at a capacitor value output line 56 will stay low under influence of the earthed transistor 52. However, as soon as the discharge signal falls to a voltage 58 which is lower than the bias threshold at the base of the transistor 52, the transistor 52 will turn off and the capacitor value signal 54 is raised at 60 by means of a pull-up resistor 62 to a voltage which corresponds to the voltage on the logic line 14. The time T between termination of the test pulse 36 and the raising of the capacitor value line 56 is representative of the energy storing capabilities of the capacitor 26, in that it represents the time taken for the discharge signal to drop below the bias threshold of the transistor 52. Should the capacitor have broken free, for instance, then the time T will be extremely short. In the event of the load 30 having broken free, the capacitor value line will be held permanently high as soon as the logic power line is raised.

Referring now to Figure 3, the capacitor value line 56 is linked to the D input of a D-type flip-flop 64, which is used to sense the value of the capacitor 26 and to provide a clock inhibit signal to a local oscillator in the event of the load 30 or the capacitor 26 being faulty. The local oscillator is an on-board oscillator which is used to generate a time reference to calculate the timing delay prior to detonation.

The oscillator is a free running imprecise oscillator which is incorporated into the logic circuitry 24. The frequency of the oscillator is fed back to the central controller for calibration during the programming phase. In the event of a detonator being faulty, a reliable method of passing this information on to the controller is to suppress the oscillator on startup, thereby not providing the necessary calibration signal and allowing the controller to indicate to the operator which electronic detonator is faulty.

Referring now to Figure 3 in conjunction with Figure 5, a short time after the logic power line 14 is raised, the logic circuitry 24 generates a power-on reset pulse 68 which sets all the logic circuits to a known state. This also has the effect of resetting the D-type flip-flop 64 and a further D-type flip-flop 70. The inverted output of flip-flop 70 turns on transistor 44 to start the discharge process through the load 30, the resistors 40 and 42 and the transistor 44. A predetermined time after the power-on reset pulse 68 has been generated, a capacitor sense pulse 72 is generated by the logic circuitry 24. The capacitor sense pulse 72 travels via capacitor sense line 74 which is linked to the clock inputs of the flip-flops 64 and 70. This pulse 72 thus has the effect of strobing an inverted version of the capacitor value signal on the capacitor value line 56 through to clock inhibit line 73 at the inverting output of the flip-flop 64. Should the capacitor still have enough charge left to hold the transistor 52 on, the capacitor value line 56 will still be low and the clock inhibit line will go and remain high, as is shown at 73A, thereby enabling the oscillator to continue operation.

However, in the event of the capacitor 26 being under-rated or the load circuitry being broken, the capacitor value line 56 will already be high, and this will have the effect of holding or toggling the clock inhibit signal 73 to a low, as is indicated at 73B, which is then used to inhibit the oscillator and to upset the handshaking procedure between the electronic detonator 10 and the central controller.

The lack of clock signals arriving at the central controller will indicate to the central controller that a fault exists in respect of the electronic detonator in question.

In order to allow for long operation of the detonator circuitry using the energy stored in the capacitor 26, it is necessary to reduce the power draining from the capacitor 26 to an absolute minimum after the testing procedure. For this reason, the D-type flip-flop 70 is also toggled by the capacitor sense line 74. The inverting output of the flip-flop 70 is connected to the base of the low power switch 44, which is in the form of a transistor. Toggling of the flip-flop 70 will thus cause the transistor 44 to be turned off, thereby minimizing drainage through the resistors 40 and 42 when the circuit is not in use. As a consequence, the discharge signal 46 rises to and remains at the remaining voltage of capacitor 26, and the capacitor value signal 54 is raised to the voltage on the logic line 14. Gradual discharge of the capacitor 26 occurs via the leakage resistance of the capacitor. Blocking diodes 78 and 80 prevent any high voltage from the detonator power line 12 from flowing back into the logic power line 14. A pull-up resistor 82 ensures that the capacitor value line 56 is pulled up to the voltage on th logic power lin 14 when one or both of th transistors 52 and 44 are ff.

Figure 6 is a self-explanatory truth tabl indicating the different fault conditi ns which may arise in the capacitor and th load, and the effect of these fault conditi ns n th clock inhibit lin .

Th fault protection circuitry may be incorporated into th integrat d circuits forming l ctronic d tonators, th reby providing a means for safely monitoring both the performance of th capacitor and of th load before

blasting takes place. This avoids th consequ nc f failure of th lectronic detonators by allowing for th ir timely replacement during th testing process.

Naturally, the testing r fault d tection circuitry f th inv nti n is not confined for use in th particular timing apparatus, but may be used to test th operation f any load and any capacitor which is arranged to discharge into that load for the purposes of detonation or the like.

Claims

1. A testing circuit characterised in that the testing circuit is arranged to test the operability both of a load (30) and of a charge storage device (26) incorporated into a main circuit (10) and being arranged to discharge into the load for detonation of the load, the testing circuit comprising:
   a) signal routing means (12) for routing a test signal (36) from a signal generator (21) for storage in the charge storage device (26);
   b) discharge means (24,40,42,44) for allowing the charge storage device (26) to provide a discharge signal (46) by discharging through the load the charge derived from the test signal;
   c) monitoring means (52) for monitoring at least one of the parameters of the discharge signal (46), and
   d) inhibiting means (64,73) responsive to the monitoring means (52) for inhibiting operation of the main circuit in the event of at least one of the monitored parameters falling outside predetermined limits (58), the limits being determined with reference to the operability both of the load (30) and of the charge storage device (26).

2. A testing circuit according to claim 1 characterised in that the monitoring means comprises a first switch (52) which is arranged to be operated by the discharge signal (46), the first switch receiving a monitoring signal (51) a predetermined time (S) after the test signal (38), and having an output (56) for delivering a discharge value signal (60) in response to the discharge signal (46) falling below a threshold value (58) which operates the first switch.

3. A testing circuit according to either one of the preceding claims characterised in that the inhibiting means includes latching means (64) for latching the output from the monitoring means (52).

4. A testing circuit according to any one of the preceding claims characterised in that the discharge means includes a second switch (44) connected along a discharge path and first control means (70) for controlling operation of the second switch (44), the control means being arranged to open the second switch once the testing circuit has operated, thereby preventing further discharge of the charge storage device (26) through the discharge means.

5. A testing circuit according to any one of the preceding claims characterised in that the monitoring means further includes means (24) for providing a first signal (68) for causing the discharge means (40,42,44) to commence discharging the charge storage device (26), means (24) for providing a second signal (72) a fixed time after the first signal (68), and means (64) responsive to the second signal (72) for controlling the inhibiting means in response to the voltage of the discharge signal at said fixed time.

6. A testing circuit according to any one of the preceding claims characterised in that at least part of the testing circuit is incorporated into an electronic detonator (10), which is linked, together with similar detonators, to a central controller (21) via a harness (11).

7. A testing circuit according to claims 2 and 6 characterised in that both the test signal (36) and the monitoring signal (51) are generated at the controller and transmitted via respective separate detonator power (12) and logic power (14) lines.

8. A method of testing the operability both of a load (30) and of a charge storage device (26) incorporated in a main circuit (10) and arranged to discharge into the load, characterised in that the method includes th st ps of
   a) gen rating a first test signal (36);
   b) storing the first test signal in th charg storag device (26);
   c) providing a discharge signal (46) by allowing th charg storage device (26) to discharg via th load;
   d) monitoring at least one of the paramet rs of th discharg signal (46); and

e) inhibiting the operation of th circuit in the ev nt of at least one of th m nit red parameters falling outside pred t rmined limits (58).

9. A m thod according to claim 8 characterised in that th test signal (36) is of such a magnitud and durati n that it is not capable of activating r d tonating th l ad (30) on discharging through th load.

10. A method according to either one of claims 8 or 9 characterised in that the parameters which are monitored include the voltage of the discharge signal and relate to the rate of discharge of the charge storage device (26), the rate of discharge being a function of an RC time constant, where C is the capacitance of the capacitor (26) and R includes the resistance of the load (30).

11. A method according to any one of claims 8 to 10 characterised in that it includes the steps of allowing the discharge signal (46) to operate a first switch (52), generating a monitoring signal (51) and supplying it to the first switch, a predetermined time (S) after the first test signal (38), and monitoring a discharge value signal as an output from the switch.

12. A method according to any one of claims 8 to 11 characterised in that the main circuit (10) forms part of an electronic detonator (10), and which includes the step of programming the electronic detonator with timing signals from a remote controller (21) in the event of the monitored parameters falling within predetermined limits, charging the charge storage device (26) from the remote controller, and allowing the charge storage device to detonate the load (30).

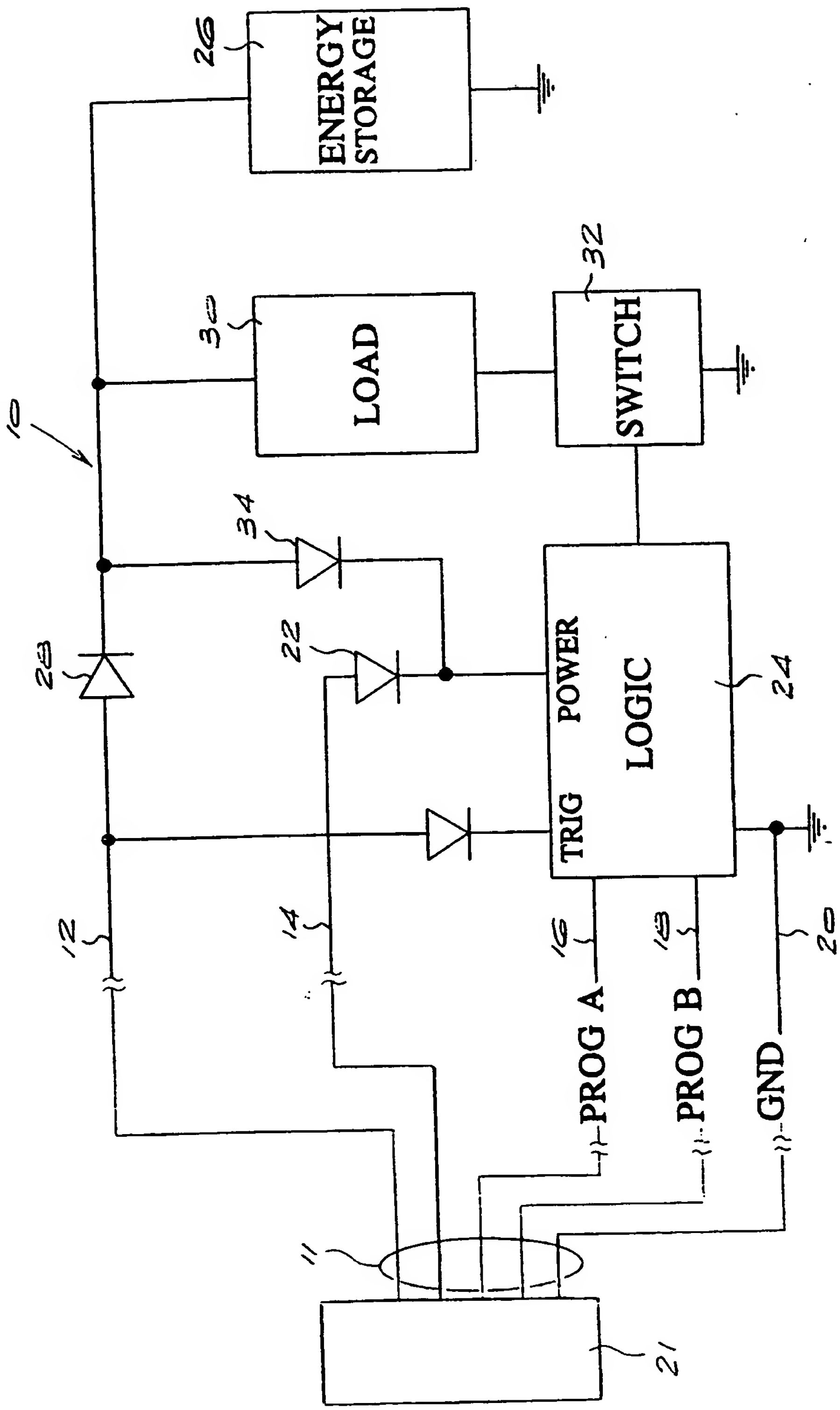

ENERGY STORAGE
26
LOAD
30
SWITCH
32
10
34
28
22
POWER
LOGIC
TRIG
24
12
14
16
18
20
PROG A
PROG B
GND
11
21

FIG.1

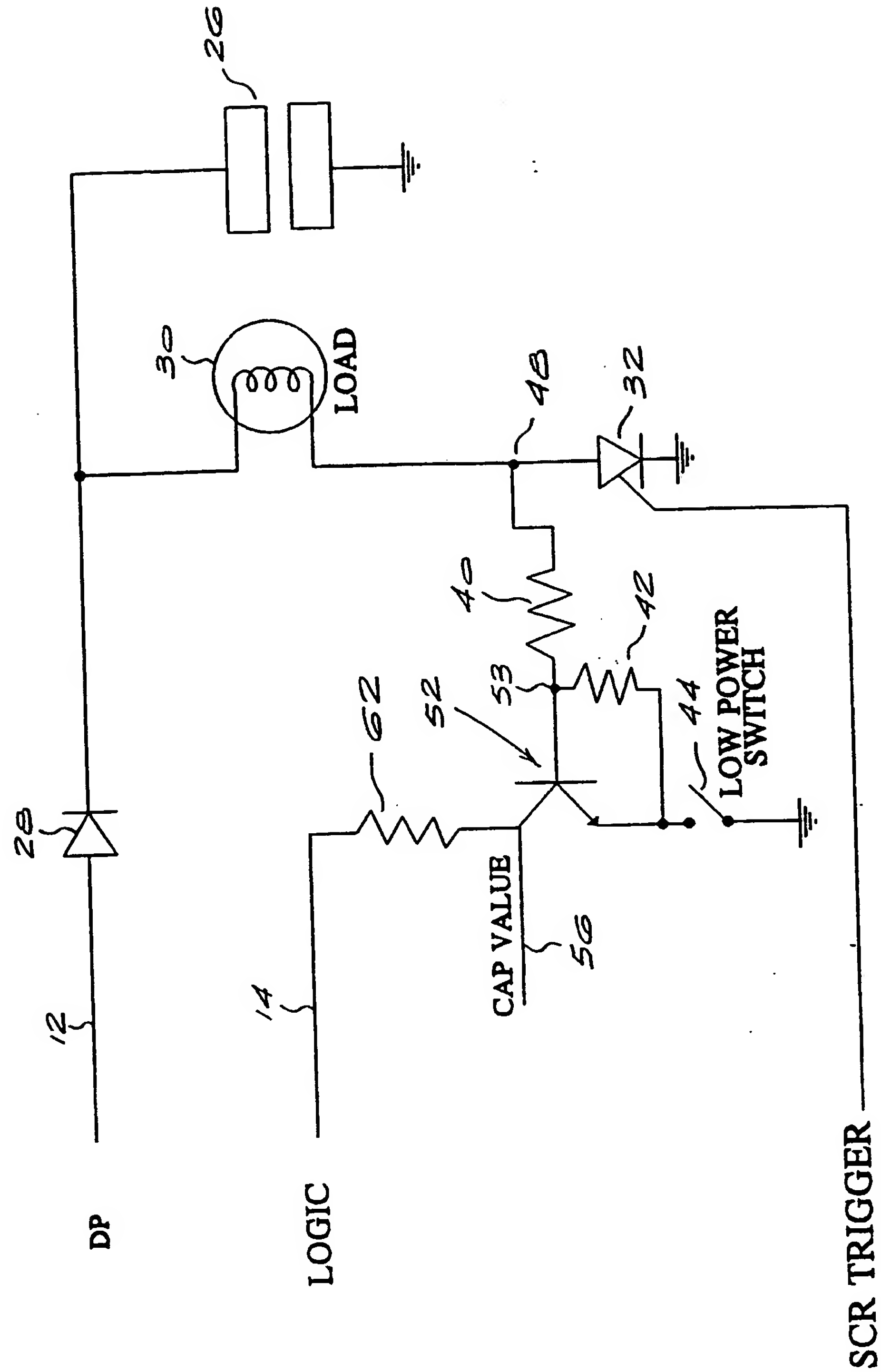

DP
12
28
LOGIC
14
62
CAP VALUE
56
52
53
40
42
44
LOW POWER SWITCH
48
30
LOAD
26
32
SCR TRIGGER

FIG.2

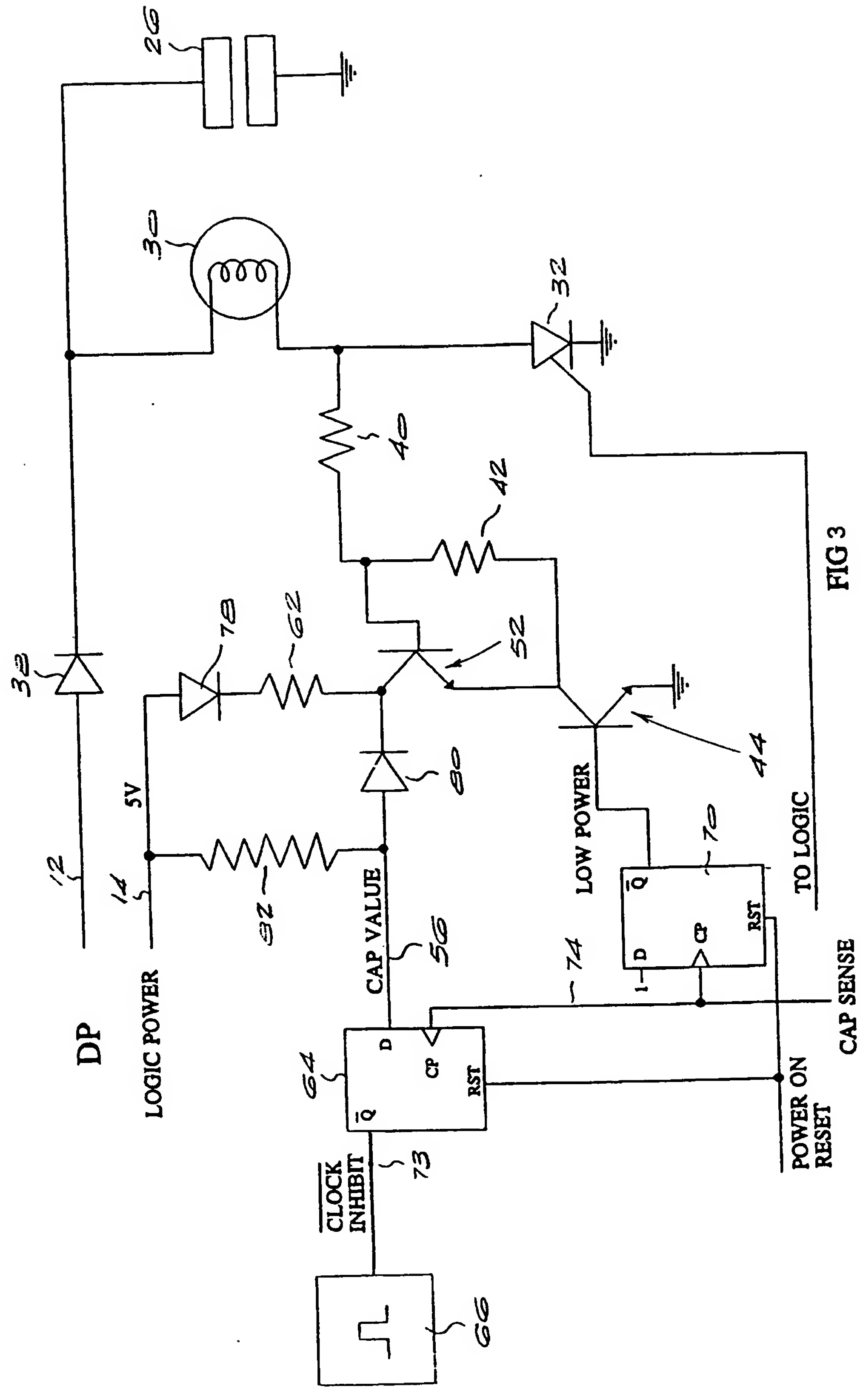

DP
LOGIC POWER
5V
CAP VALUE
LOW POWER
TO LOGIC
CAP SENSE
POWER ON RESET
CLOCK INHIBIT
D
CP
RST
Q̄
12
14
26
30
32
40
42
44
52
56
62
64
66
70
73
74
78
80

FIG 3

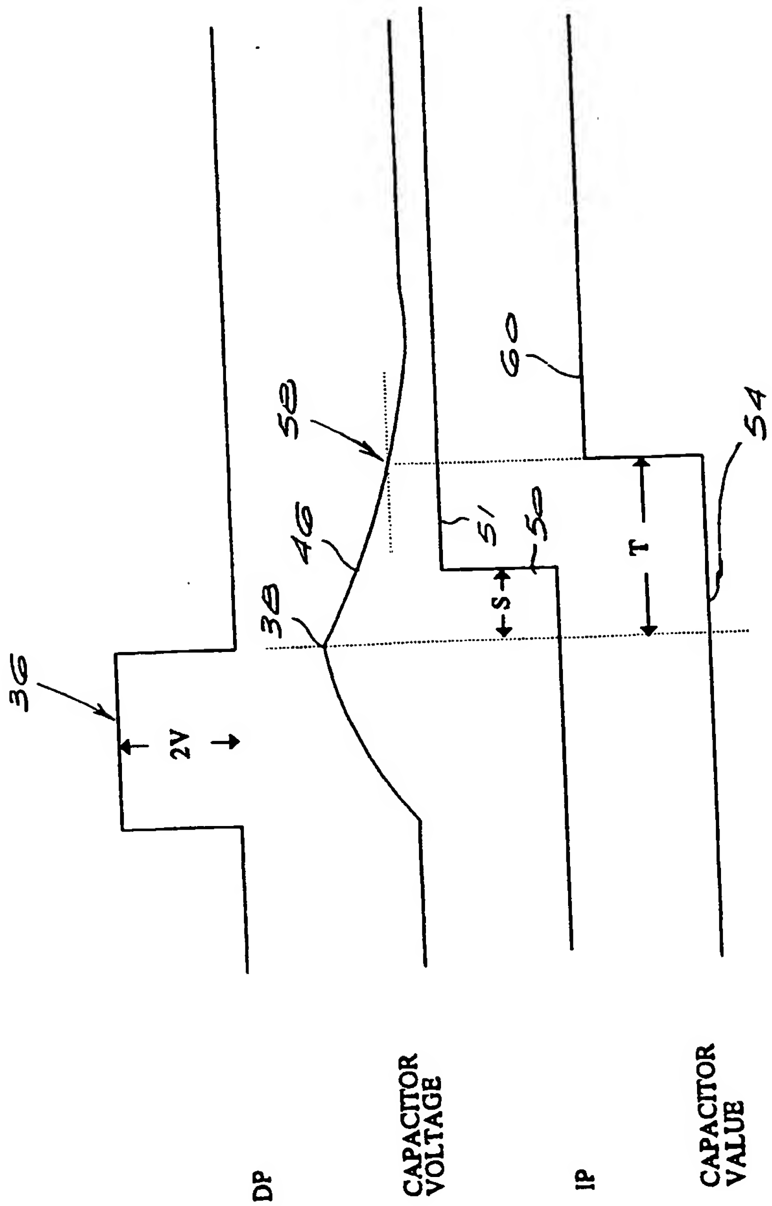

DP
CAPACITOR VOLTAGE
IP
CAPACITOR VALUE
2V
S
T
36
38
46
58
51
50
60
54

FIG.4

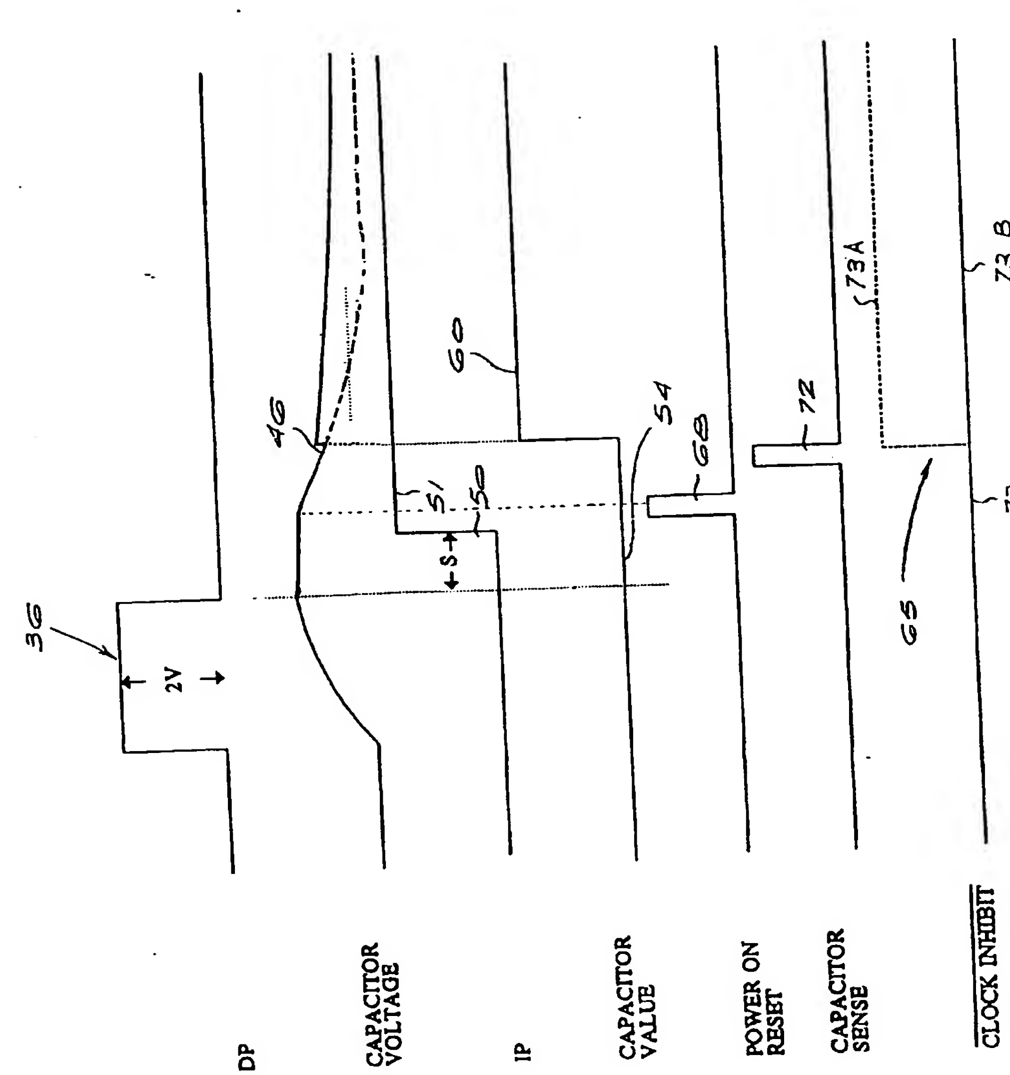

36
2V
46
S
51
50
54
60
68
72
73A
73B
73
65
DP
CAPACITOR VOLTAGE
IP
CAPACITOR VALUE
POWER ON RESET
CAPACITOR SENSE
$\overline{\text{CLOCK INHIBIT}}$

FIG.5

CAPACITOR	LOAD	CLOCK INHIBIT
CORRECT	CONNECTED	NOT INHIBITED
TOO SMALL	CONNECTED	INHIBITED
TOO LARGE	CONNECTED	NOT INHIBITED
CORRECT	NOT CONNECTED	INHIBITED
TOO SMALL	NOT CONNECTED	INHIBITED
TOO LARGE	NOT CONNECTED	INHIBITED
SHORT CIRCUIT	CONNECTED	INHIBITED
OPEN CIRCUIT	CONNECTED	INHIBITED

FIG. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 1177

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	WO-A-90 01670 (RITMANICH) * page 6 - page 9 * ---	1,8	F42C21/00 G01R31/02
A	EP-A-0 296 015 (ALKAN) -----		
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			F42C G01R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 March 1994	Hoornaert, W

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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